Pipeline Scalable Architecture for High Density and High Speed Content Addressable Memory (CAM)

Abstract

The Inventions divide the entire CAM block into many identical small sub-block and then symmetrically place them. Divide them into four quadruple ,then in each quadruple place them in equal row and column. the address, data bus are routed symmetrically into the center first and then to each quadruple, then to each column in each quadruple and then into each sub-block. Address decoding, Content matching in each sub-block, priority encoding, hit result reading out in different cycle . In this way, each cycle time can be short , and the throughput of CAM matching can be increased. In this design the power can be reduced. Each sub-blocks are identical. The logical interface among sub-block in each column are identical. The design is scalable.